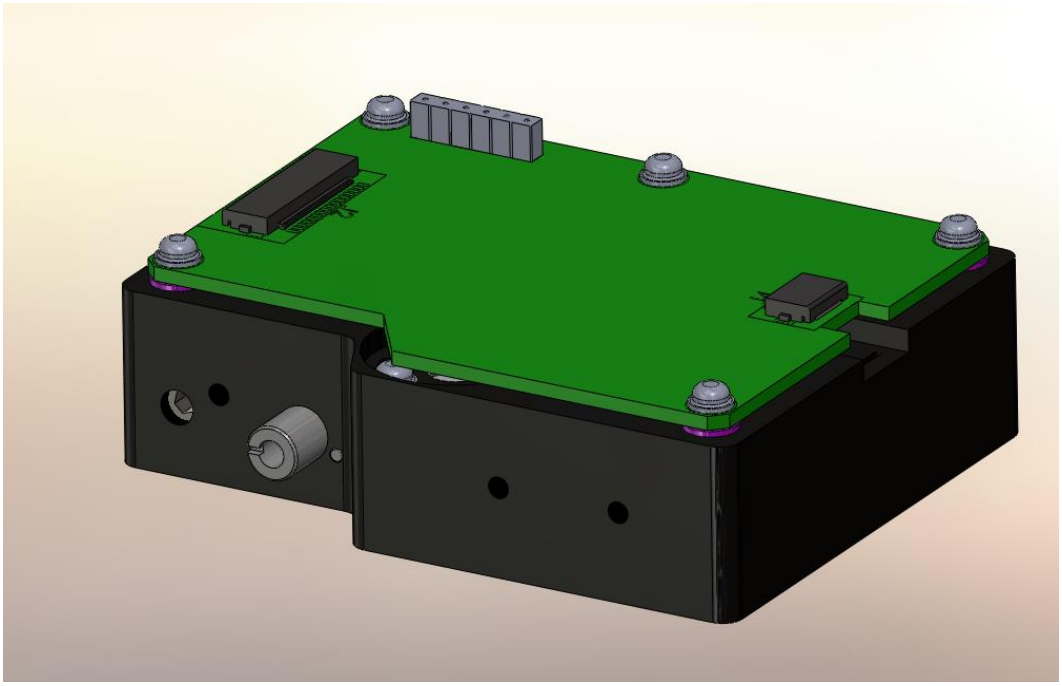
Ocean Optics
A HALMA COMPANY

830 Douglas Ave.
Dunedin, FL 34698
+1 727-733-2447
www.OceanOptics.com

# EMBED2000+ Data Sheet

## Description

The Ocean Optics EMBED2000+ Spectrometer includes the linear CCD-array optical bench, plus all the circuits necessary to operate the array and convert to a digital signal. The result is a compact, flexible system, with no moving parts, that's easily integrated as an OEM component.



The EMBED2000+ Spectrometer is a unique combination of technologies providing users with both an unusually high spectral response and high optical resolution in a single package. The electronics have been designed for considerable flexibility in connecting to various modules as well as external interfaces. The information included in this guide provides detailed instructions on the connection and operation of the EMBED.

The detector used in the EMBED spectrometer is a high-sensitivity 2048-element CCD array from Sony, product number ILX511B. (For complete details on this detector, visit Sony's web site at www.sony.com. Ocean Optics applies a coating to all ILX511 detectors, so the optical sensitivity could vary from that specified in the Sony datasheet).

The EMBED operates from a single +3.3VDC supply.

# Features

- ILX511B Detector
  - High sensitivity detector
  - Readout Rate: 2.4MHz
- Optics
  - An optical resolution of ~0.3nm (FWHM)
  - A wide variety of optics available
    - 14 gratings, plus Grating #31for the XR version
    - 6 slit widths
    - 3 detector coatings
    - 6 optical filters
- Electrical Performance
  - 16 bit, 3.3MHz A/D Converter
  - Integration times from 1ms to > 60s
- EEPROM storage for
  - Wavelength Calibration Coefficients
  - Linearity Correction Coefficients
- Built-in triggering for easy synchronization to an event from 1 of 2 pin sources

# Specifications

| Specifications | Criteria |
|---|---|
| Absolute Maximum Ratings: | |
| $V_{CC}$ (System Power) | -0.5 VDC to +4.7 VDC |
| I/O | -0.5 VDC to +3.5 VDC, 10 mA (maximum) |
| Physical Specifications: | |
| Physical Dimensions | 89.1 mm x 63.3 mm x 34.4 mm |
| Weight | 190 g |
| Power: | |
| Supply voltage | 2.65 to 3.6 VDC |
| Power requirement | 100 mA @ 3.3 VDC |
| Recommended Operating Conditions | |
| Vcc (System Power) | +3.3 VDC |
| I/O (except for ContStrobe and SingleStrobe) | 0 VDC to +3.3 VDC, 10 mA (maximum) |
| ContStrobe, SingleStrobe | 0 VDC to +5.0 VDC, 10 mA (maximum) |
| Spectrometer: | |
| Design | Asymmetric crossed Czerny-Turner |
| Focal length (input) | 42mm |
| Focal length (output) | 68mm (75, 83, and 90mm focal lengths are also available) |
| Input Fiber Connector | SMA 905 |
| Gratings | 14 different gratings, plus Grating #31 for the XR version |
| Entrance Slit | 5, 10, 25, 50, 100, or 200 µm slits. (Slits are optional. In the absence of a slit, the fiber acts as the entrance slit.) |
| Detector | Sony ILX511B CCD |
| Filters | 2nd and 3rd order rejection, long pass (optional) |
| Spectroscopic: | |
| Integration Time | 1 ms – >60 sec |
| Dynamic Range | 1300:1 (per pixel) |
| Signal-to-Noise | 250:1 single acquisition |
| Readout Noise (single dark spectrum) | 50 counts RMS, 300 counts peak-to-peak |
| Resolution (FWHM) | 0.03 – 10.0 nm varies by configuration (see www.Oceanoptics.com for configuration options) |
| Spectrometer Channels | One |
| Environmental Conditions: | |
| Temperature | -30° to +70° C Storage & -10° to +50° C Operation |
| Humidity | 0% - 90% non-condensing |

# Internal Operation

## Pixel Definition

A series of pixels in the beginning of the scan have been covered with an opaque material to compensate for thermal induced drift of the baseline signal. As the EMBED warms up, the baseline signal will shift slowly downward a few counts depending on the external environment. The baseline signal is set around 2600 counts at the time of manufacture. The following is a description of all of the pixels, both as they exist on the detector and as they are actually read from the FPGA.

**Pixels on the Device**

| Pixel | Description |
|---|---|
| 0–12 | Not usable |
| 13–30 | Optical black pixels |
| 31–32 | Not usable |
| 33–2080 | Optical active pixels |

Note that the EMBED only digitizes pixels 13 through 2060. During readout the first pixel is the first optical black pixel.

# CCD Detector Reset Operation

At the start of each integration period, the detector transfers the signal from each pixel to the readout registers and resets the pixels. The total amount of time required to perform this operation is ~3 µs. When using trigger mode the user needs to account for this time delay when the pixels are optically inactive.

# Communication and Interface

## Initialization

On power up the FPGA loads its program contents from a dedicated external EEPROM that configures the FPGA. After configuration the X_RESET pin must be strobed from low-high-low for a minimum of 1us to initiate a global reset. It is essential that the controlling program waits for FPGA configuration before initiating the global reset.

The typical time needed for the attached EEPROM to configure the FPGA after 3.3V power-on is 100ms. After issuing the X_RESET pulse an additional 100ms delay is needed for the internal clocks to stabilize.

## Interface

The EMBED detector board contains a Xilinx® FPGA to handle detector clocking and analog-to-digital results of pixel information. The FPGA is controlled via an industry standard SPI bus to write and read all operating parameters as well as retrieving spectral data from the spectrometer. Additionally, one Microchip® 25AA040A EEPROM and an Analog Devices® ADT7301 precision centigrade temperature sensor are available on separate SPI chip selects for storage of calibration data and detector temperature monitoring.

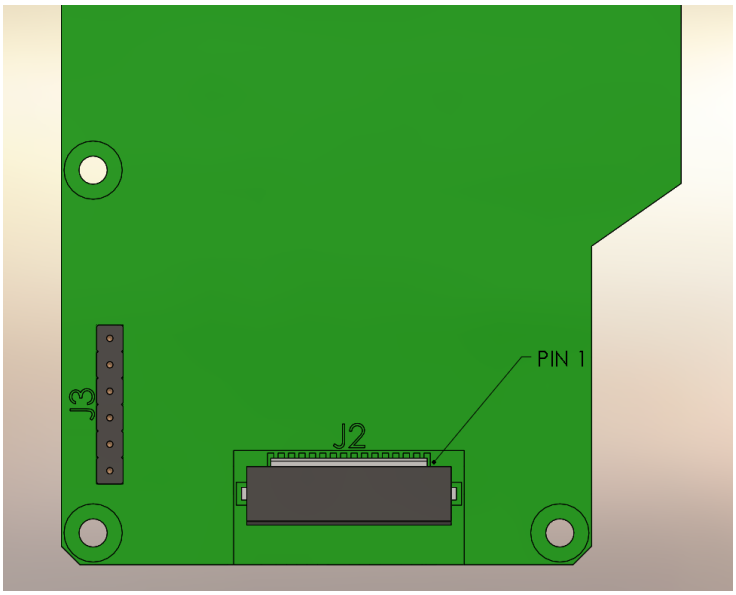
All chip select SPI devices are designed to operate on the same clock phase and polarity.

All signals required for communication via the SPI bus and control of the spectrometer are available on a 16-pin Hirose FFC 1mm connector. The pinout and signal descriptions are provided in the table below. The part number of the Hirose connector is: FH12-16S-1SH(55)

| Pin # | Signal Name | In/Out | Rating | Description |
|---|---|---|---|---|
| 1 | GND | N/A | N/A | System ground |
| 2 | 3.3V | Input | 3.3V | System power |
| 3 | FIFO_CS | Input | 3.3V | FIFO Chip Select |
| 4 | X_RESET | Input | 3.3V | FPGA async. global reset |
| 5 | FIFO_RST | Input | 3.3V | Acquisition source |
| 6 | PIXEL_RDY | Input | 3.3V | Pixel data ready |
| 7 | MISO | Output | 3.3V | SPI data from slave |
| 8 | MOSI | Input | 3.3V | SPI data to slave |
| 9 | SPI_CLK | Output | 3.3V | SPI clock |
| 10 | SPI_CS | Input | 3.3V | FPGA chip select |
| 11 | ADT_CS | Input | 3.3V | Temperature IC chip select |
| 12 | E2_CS | Input | 3.3V | Calibration EEPROM select |
| 13 | Trigger | Input | 3.3V | Acquisition event trigger |
| 14 | ContStrobe | Output | 5V | Free running clock |
| 15 | SingleStrobe | Output | 5V | Integration synchronous clock |
| 16 | NC | N/A | N/A | Manufacturing use only |

**Note**

The location of signal pin 1 is different from the connector datasheet. Please refer to the diagram below for the explicit location.




## FPGA Communication

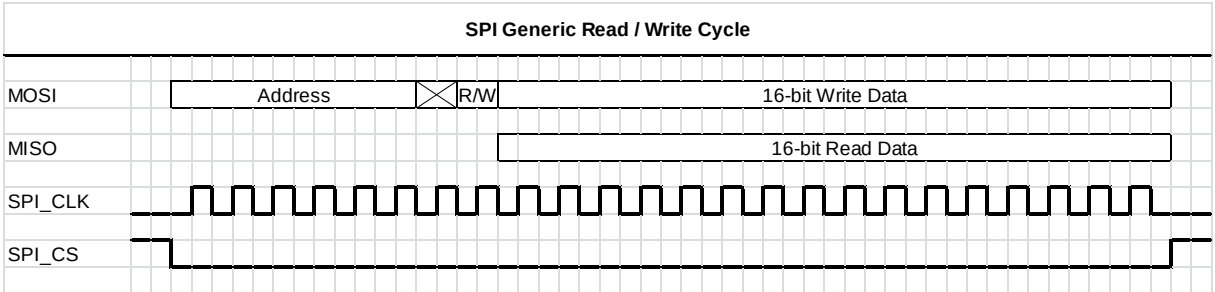
The SPI bus is the I/O communication link between the controlling device and FPGA. The FPGA is considered the slave device and handles up to a 16MHz SPI clock for decoding MOSI bitstreams. Data on MOSI is clocked in on the falling edge of the SPI clock, while data out to MISO is latched on the rising edge.

## SPI Communication Examples

Each read and write transfer is 24 clock pulses total consisting of 6 address bits, a null bit, a R/W bit 0/1 respectively, and 16 data bits.

The MOSI bitstream is decoded on the rising edge of each SPI_CLK. All values returned from a read cycle transition on the falling edge of SPI_CLK.

Below is an example of a single generic SPI read/write cycle. Information on MISO and MOSI is ordered most significant bit first.



## SPI Registers

Below is a table containing the available register addresses for FPGA configuration and operation.

| | Address | Capability | Default Values |
|---|---|---|---|
| FPGA_VERSION | 0x04 | Read | Version Specific |
| FPGA_COUNTBASE | 0x08 | Read/Write | 0x0000 |
| FPGA_STRBCOUNT | 0x0C | Read/Write | 0x0000 |
| FPGA_INTCLOCK | 0x18 | Read/Write | 0x0006 |
| FPGA_SSLOWDELAY | 0x38 | Read/Write | 0x0003 |
| FPGA_SSHIGHDELAY | 0x3C | Read/Write | 0x0000 |
| FPGA_LAMPENABLE | 0x40 | Read/Write | 0x0000 |
| FPGA_OFFSETVALUE | 0x5C | Read/Write | 0x0000 |
| FPGA_MAXSATVALUE | 0x68 | Read/Write | 0x0000 |

## SPI Register Description

FPGA_VERSION - 0x04

A read from this register provides the current FPGA configuration version.

FPGA_COUNTBASE - 0x08

This register divides provides a base frequency counter for the Continuous strobe function. CS_BasePeriod = FPGA_COUNTBASE / 48MHz

FPGA_STRBCOUNT - 0x0C

This register uses the COUNTBASE register at address 0x08 to form the Continuous Strobe signal.

ContStrobe = (FPGA_STRBCOUNT + 1) * CS_BasePeriod

FPGA_INTCLOCK - 0x18

This register is used to generate the detector integration time represented in milliseconds. Values of 1 to 0xFFFF are used for integration times of 1ms and 65.535s.

FPGA_SSLOWDELAY -0x38

This value corresponds to the time delay that the SingleStrobe signal goes low after the start of an integration time.

FPGA_SSHIGHDELAY -0x3C

This value corresponds to the time delay that the SingleStrobe signal goes high after the start of an integration time.

Note: The value in LOWDELAY must be higher than HIGHDELAY in order for a strobe to be present.

FPGA_LAMPENABLE -0x40

The least significant bit of this register is the global enable (1) and disable (0) for both the Continuous Strobe and Single Strobe functions present on Hirose Pin 14 and 15, respectively.

FPGA_OFFSETVALUE -0x5C

This register is a calibration value for normalizing detector baselines.

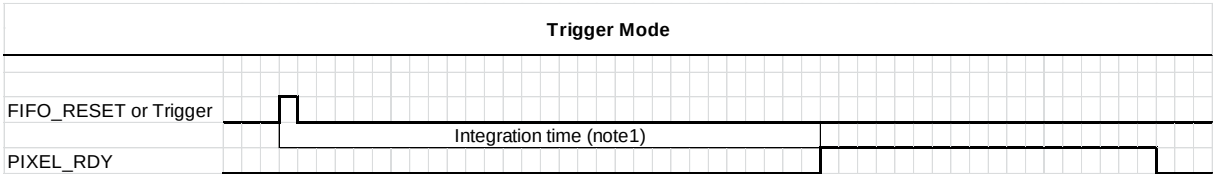
FPGA_MAXSATVALUE -0x68

This register is a calibration value for normalizing detector gain.

Data for both register addresses 0x5C and 0x68 are obtained from the SPI calibration EEPROM. This value is static and needs to be written only once following an X_RESET event.

## Spectral Acquisition

The following diagram shows the two possible sources for triggering an acquisition: FIFO_RESET or Trigger. Both are identical in functionality. Once an acquisition is in progress, the spectrometer will lock out any additional triggers from either source until the defined integration time has expired.



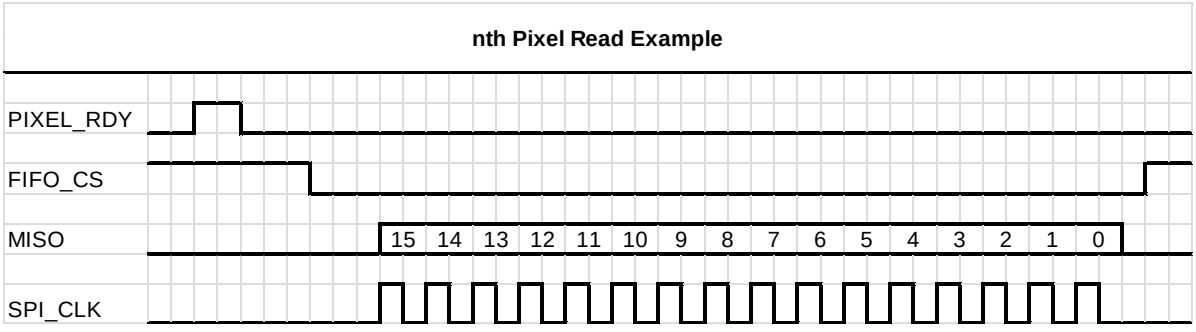

Note 1: The FPGA has a set up time of 840ns from the time the acquisition source goes high to when the ILX511B starts to transfer the charge to the readout array. This gives a total delay of 3.840us from the trigger source until the start of integration.

When the integration time has expired and the first pixel is available in memory, PIXEL_RDY will assert high and contents are ready to be read as described in “Reading Pixel Data”.

## Reading Pixel Data

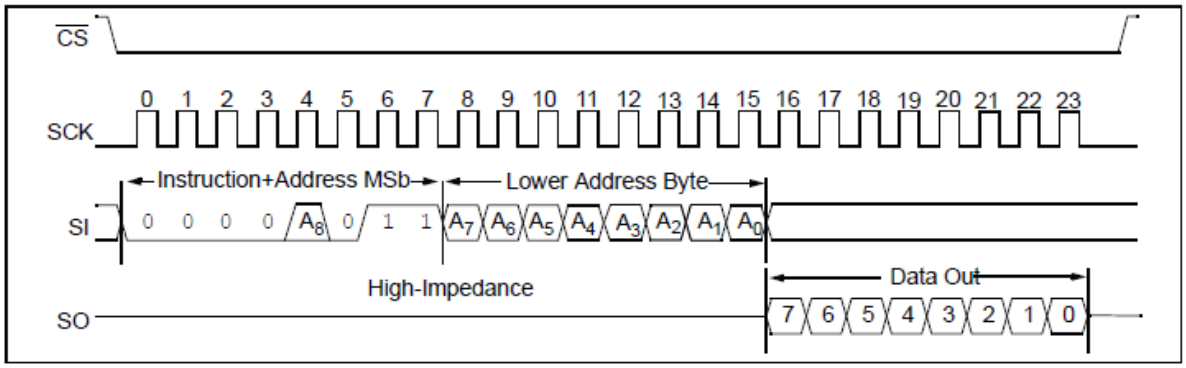
The following diagram shows how to receive spectral data over SPI. PIXEL_RDY is reported by the FPGA once an unread pixel is ready in the FIFO. To read the FIFO contents FIFO_CS is brought low to shift FIFO data to an internal buffer awaiting SPI transfer.

This process is repeated for the entire 2048 pixel FIFO, however it is not required to read out all 2048 pixels. The read process can be aborted and a new scan initiated by issuing a FIFO_RESET or External Trigger.



## EEPROM SPI Read

The EMBED contains a separate 4kb SPI EEPROM that is populated with spectrometer calibration data. Below is an example for a single byte read. Please see the device datasheet for complete timing and operation information. The chip select is E2_CS located on pin 12.




Starting at address 0x000, the calibration data is parsed as follows:

| | |
|---|---|
| COEF_SERIAL | 0x000 – 0x00F |
| COEF_ICEP | 0x010 – 0x01F |
| COEF_C1 | 0x020 – 0x02F |
| COEF_C2 | 0x030 – 0x03F |
| COEF_C3 | 0x040 – 0x04F |
| COEF_STRAY | 0x050 – 0x05F |
| COEF_NL0 | 0x060 – 0x06F |
| COEF_NL1 | 0x070 – 0x07F |
| COEF_NL2 | 0x080 – 0x08F |
| COEF_NL3 | 0x090 – 0x09F |
| COEF_NL4 | 0x0A0 – 0x0AF |
| COEF_NL5 | 0x0B0 – 0x0BF |
| COEF_NL6 | 0x0C0 – 0x0CF |
| COEF_NL7 | 0x0D0 – 0x0DF |
| COEF_NLORDER | 0x0E0 – 0x0EF |
| COEF_CONFIG1 | 0x0F0 – 0x0FF |
| COEF_CONFIG2 | 0x100 – 0x10F |
| COEF_OFFSET | 0x110 – 0x11F |

COEF_SERIAL contains ASCII bytes of the spectrometer serial number.

COEF_ICEP through COEF_NL7 are stored in ASCII format and are described using scientific notation. For example, -0.00000000000000123 is interpreted as (-1.23e-15) and is stored as (2D 31 2E 32 33 65 2D 31 35). ICEP is the x-axis intercept, through C3 as the third order coefficient to convert discrete pixels into wavelengths.

COEF_NL0 – 7 are coefficients for a $7^{th}$ order polynomial to correct for detector non-linearity.

COEF_CONFIG1 and CONFIG2 are set by Ocean Optics and are for manufacturing use only.

COEF_OFFSET is a special case that contains information that must be passed down to the FPGA during initialization for unit-to-unit consistency. The coefficient contains 6 bytes of information parsed in the following order:

Bytes 0 and 1 are ignored.

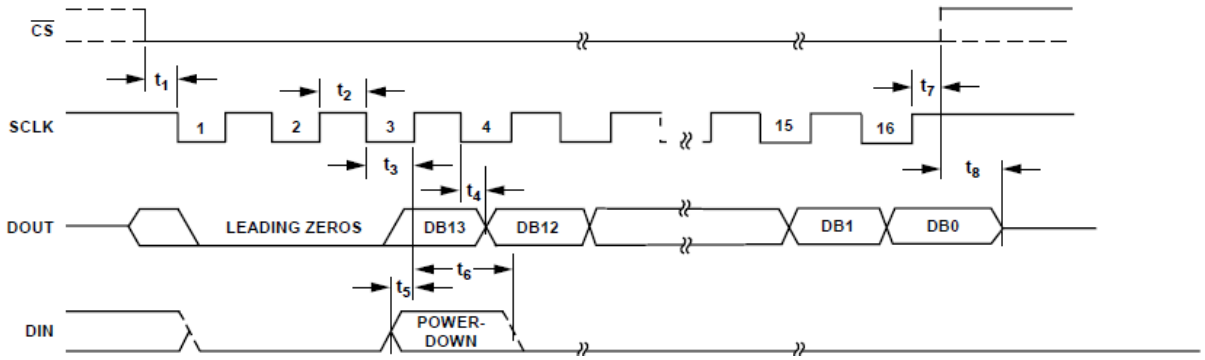
Bytes 2 and 3 are the LSB and MSB respectively for FPGA_OFFSETVALUE.

Bytes 4 and 5 are the LSB and MSB respectively for FPGA_MAXSATVALUE.

Each ILX511B has unique baseline and gain values. The information contained in COEF_OFFSET are calibration values that offer uniformity in the dark baseline and saturation value at the expense of a small amount of dynamic range.

## ADT7301 Temperature Sensor Read

Below is a diagram of one temperature read cycle. Please refer to the product datasheet for complete timing and operation information. The chip select is ADT_CS located on pin 11.



## Mechanical Information

Below are drawings describing overall dimensions and mounting locations. A .pdf format drawing is available from Ocean Optics Engineering upon request.